



Product Information

SXC-LOOP

CompactPCI® Serial • PCI Express® External Cabling

Target Side Adapter (PCIe® Gen3 x8)

Enables PCIe® Based Peripheral Cards in a CompactPCI® Serial Target System

Document No. 8745 • 9 December 2020



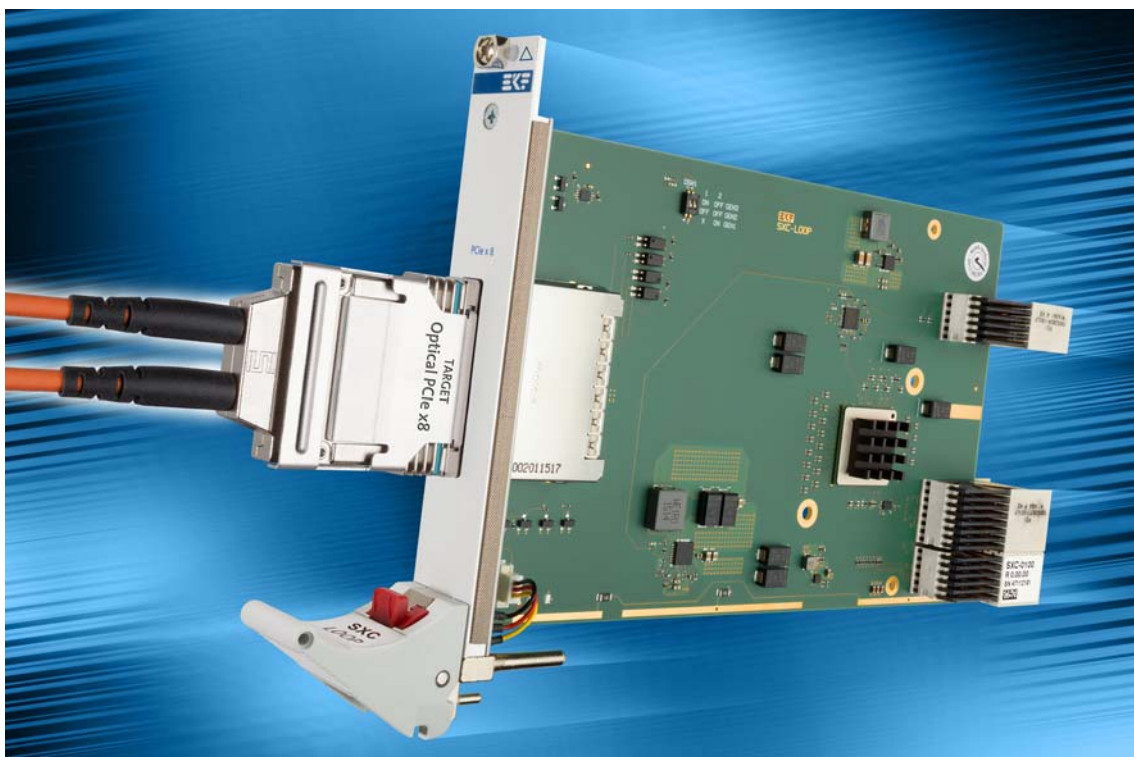
General

Most computer systems are based on the PCI Express® standard as a high speed backbone for interconnection of peripheral components with a host CPU. Typically all PCI Express® based devices are located closely in a common enclosure.

The PCI-SIG PCI Express® External Cabling Specification for Gen1 and Gen2 data transfer rates addresses extended applications, such as split-systems or I/O expansion by means of a suitable copper cable, available e.g. for a x8 PCI Express® link, up to 7m length. When used with an AOC (Active Optical Cable), distances of up to 300m can be bridged between host and target systems. Beyond the PCI-SIG cabling specification, the Samtec PCIEO series of AOC addresses also Gen3 speed up to 100m.

The SXC-LOOP is a target system adapter card for PCIe x8 external cabling. The SXC-LOOP fits into the system slot of a CompactPCI® Serial target system backplane. The on-board packet switch is used to replicate two PCI Express® Gen3 x8 links across a 3-slot CompactPCI® Serial backplane. Thus, two CompactPCI® Serial 'fat pipe' slot cards in a target system can be controlled by the remote host system CPU, with a transfer rate of up to 64Gbps, suitable e.g. for NVMe based SSD mass storage boards or GPU cards.

The advantages of PCI Express® compared e.g. to 10Gbps Ethernet are higher data transfer speed at lower latency, and primarily merging distributed subsystems virtually into a single PCI Express® based computer assembly.



System Integration

The SXC-LOOP allows to control a CompactPCI® Serial target (downstream) system by a remote host CPU via PCI Express® external cabling. The host (upstream) system may be any computer with a PCI Express® external cabling spec conforming adapter, not necessarily a CompactPCI® Serial system.

Being mainly a powerful PCI Express® Gen3 packet switch, the SXC-LOOP is organized similar to a CompactPCI® Serial system slot controller card, however restricted to the PCI Express® resources of the CompactPCI® Serial backplane.

The SXC-LOOP is linked to the host system by a PCI Express® x8 front panel cabling connector (upstream), and delivers two PCI Express® links to its backplane connectors (downstream), for two CompactPCI® Serial 'fat pipe' peripheral cards in a target system. Both links/slots on the CompactPCI® Serial backplane are organized as Gen3 x8, for demanding boards such as SSD mass storage, GPU or FPGA cards, or high resolution camera I/O.

With the SXC-LOOP, PCI Express® based devices in the target system can be controlled by the remote host system CPU in an identical manner as its local resources.



Feature Summary

General

- ▶ PCI Express® external cabling target side adapter
- ▶ PICMG® CompactPCI® Serial (CPCI-S.0) system slot controller (PCIe resources only)
- ▶ Single Size Eurocard 3U 4HP 100x160mm²
- ▶ CompactPCI® Serial backplane connectors P1, P2, P5 for 2 PCI Express® links
- ▶ Peripheral slots organized x8/x8
- ▶ Clamshell available for extremely rugged applications e.g. ATR & conductive cooled assembly (CCA)

Cabling

- ▶ *PCI Express® External Cabling Specification* x8 connector 68-pos. (front panel)
- ▶ Full sideband support
- ▶ Suitable for CompactPCI® Serial target systems to be controlled by a remote host
- ▶ Split-systems, hybrid systems, or system expansion applications
- ▶ Suitable for any host system with PCI Express® x8 external cabling host adapter
- ▶ Copper cable assemblies 0.5m to 7m length available
- ▶ PCIe® Gen2 active optical cable assemblies (AOC) up to 300m length available (Samtec)
- ▶ PCIe® Gen3 active optical cable assemblies (AOC) up to 100m length available (Samtec)
- ▶ AOC half cable assemblies available iPass™ to MTP male/female (Samtec)
- ▶ PCIe Gen3 x8 allows for up to 64Gbps bandwidth
- ▶ PCIe Gen2 x8 allows for up to 40Gbps bandwidth

Special Features

- ▶ Gen3 PCI Express® 24-lanes packet switch on-board
- ▶ Upstream port Gen3 x8 (to host system)
- ▶ Two downstream ports Gen3 x8 (to backplane)
- ▶ CompactPCI® Serial peripheral slots organized x8/x8 Gen3
- ▶ Recommended 3-slot backplane (system slot + two 'fat pipe' slots)

Feature Summary

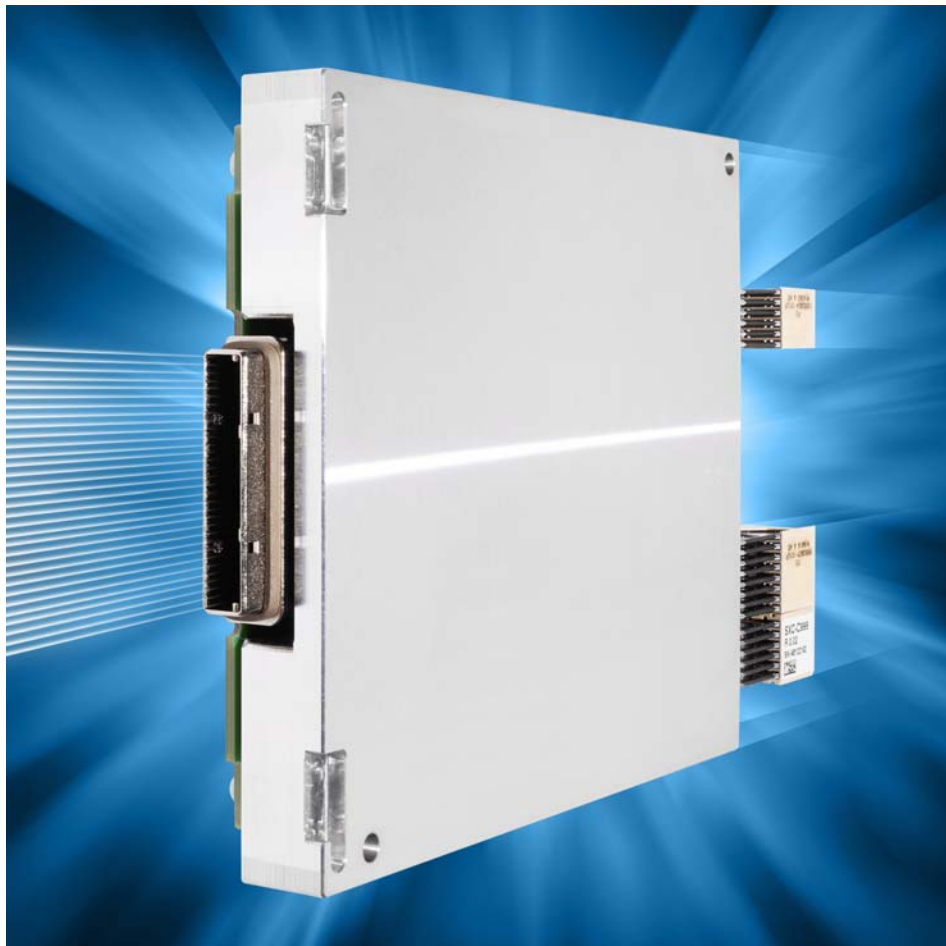
Applications

- ▶ For lowest latency at fastest speed connected systems
- ▶ Distributed computing - host to target system hierarchy
- ▶ Peer to peer computing - special TCP/IP stack (Dolphin) available
- ▶ Split-systems, hybrid systems, or system expansion applications
- ▶ Direct host to target device connection (e.g. PCIe® sed remote NVMe mass storage)
- ▶ Mating host system adapter board available for CompactPCI® Serial (SX5-STREAM)

Regulatory

- ▶ Long term availability
- ▶ Designed & manufactured in Germany
- ▶ ISO 9001 certified quality management
- ▶ Rugged solution (coating, sealing, underfilling on request)
- ▶ RoHS compliant 2002/95/EC
- ▶ Commercial and industrial temperature range
- ▶ Humidity 5% ... 95% RH non condensing
- ▶ Altitude -300m ... +3000m
- ▶ Shock 15g 0.33ms, 6g 6ms
- ▶ Vibration 1g 5-2000Hz
- ▶ MTBF 77.9 years
- ▶ EC Regulations EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1)

Clamshell Version



Theory of Operation

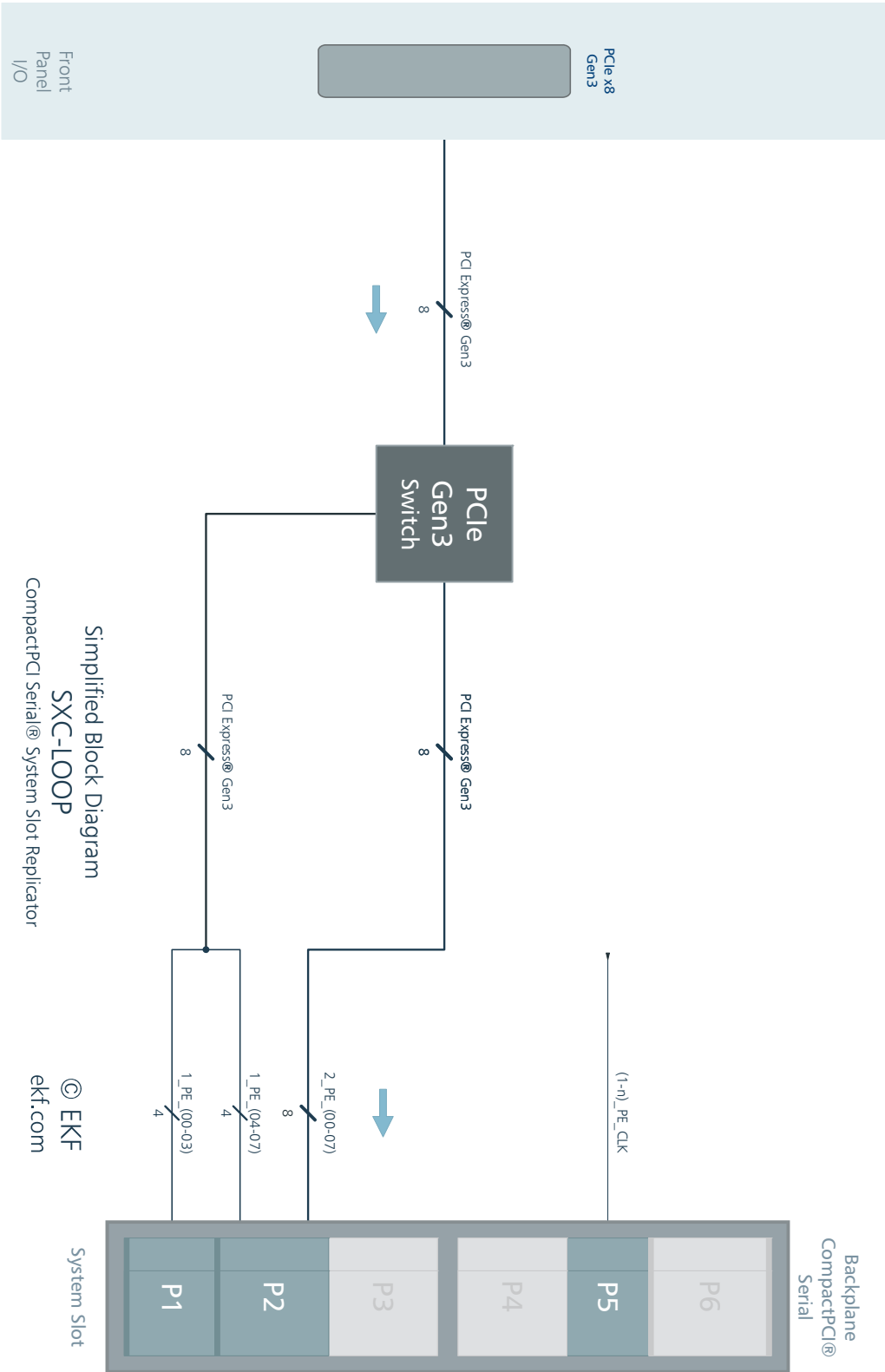
The SXC-LOOP must be inserted into the system slot of the CompactPCI® Serial target system. The PCIe x8 link derived from the front panel cabling connector is distributed across a 24-lane PCI Express® Gen3 packet switch to the CompactPCI® Serial backplane connectors P1/P2, for usage on two fat pipe peripheral slots (link width x8).

Both fat pipe (downstream) backplane slots share the upstream link (front connector) available bandwidth, i.e. up to 64Gbps in total for a Gen3 external cabling.

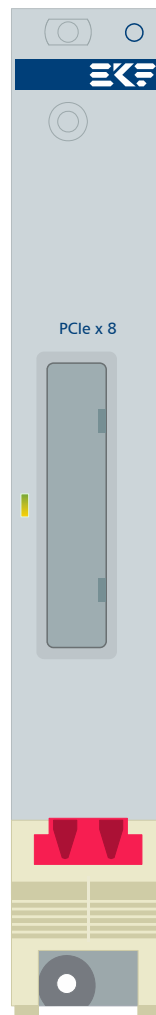
Any CompactPCI® Serial standard backplane may be used for the target system, but only the two fat pipe peripheral slots are active available.



Block Diagram



Front Panel



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SXC-LOOP

Front panel LED off - no PCIe® cable link established

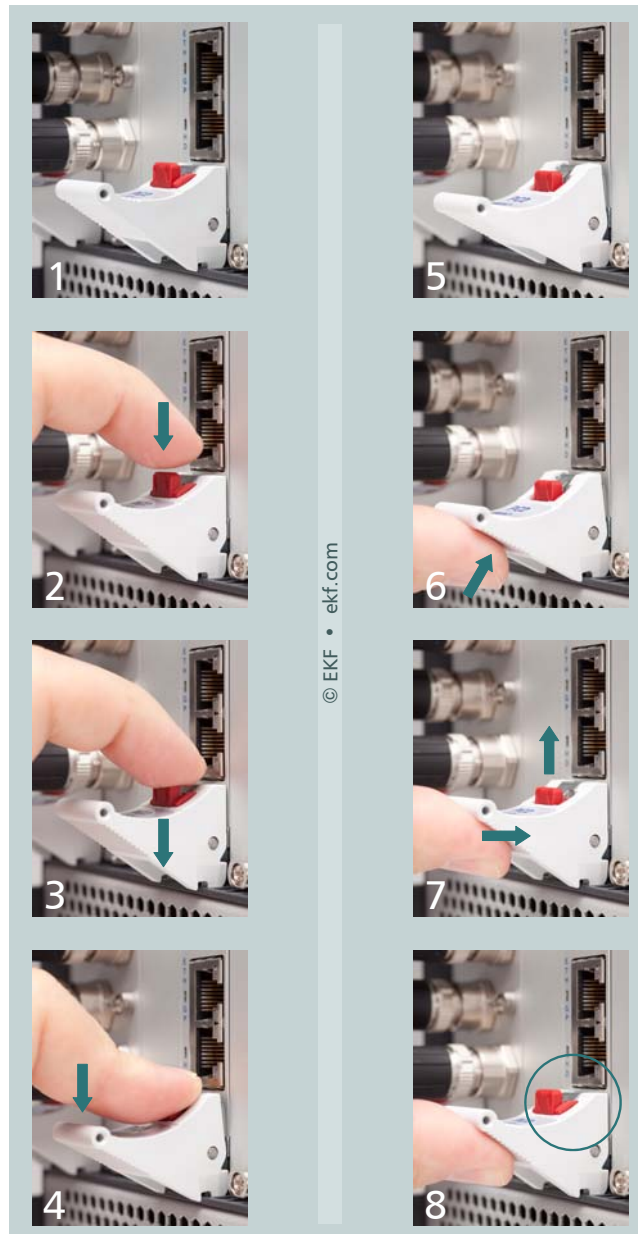
Front panel LED permanently on - PCIe® Gen3 cable link established

Front panel LED blinking 2Hz - PCIe® Gen2 cable link established

Front panel LED blinking 1Hz - PCIe® Gen1 cable link established

As result of the PCI Express® link training, links are established which are suitable for communication between both sides, i.e. host controller (e.g. SX5-STREAM) and target side adapter (SXC-LOOP). The link width can vary between 1 - 2 - 4 - 8 dependent from the host adapter, and the data transfer rate may be either 2.5GT/s (Gen1), 5GT/s (Gen2) or 8GT/s (Gen3). With respect to the SX5-STREAM host side adapter and suitable cabling and setup, the LEDs on both sides should be steady on (indicating Gen3), and the link width is x8.

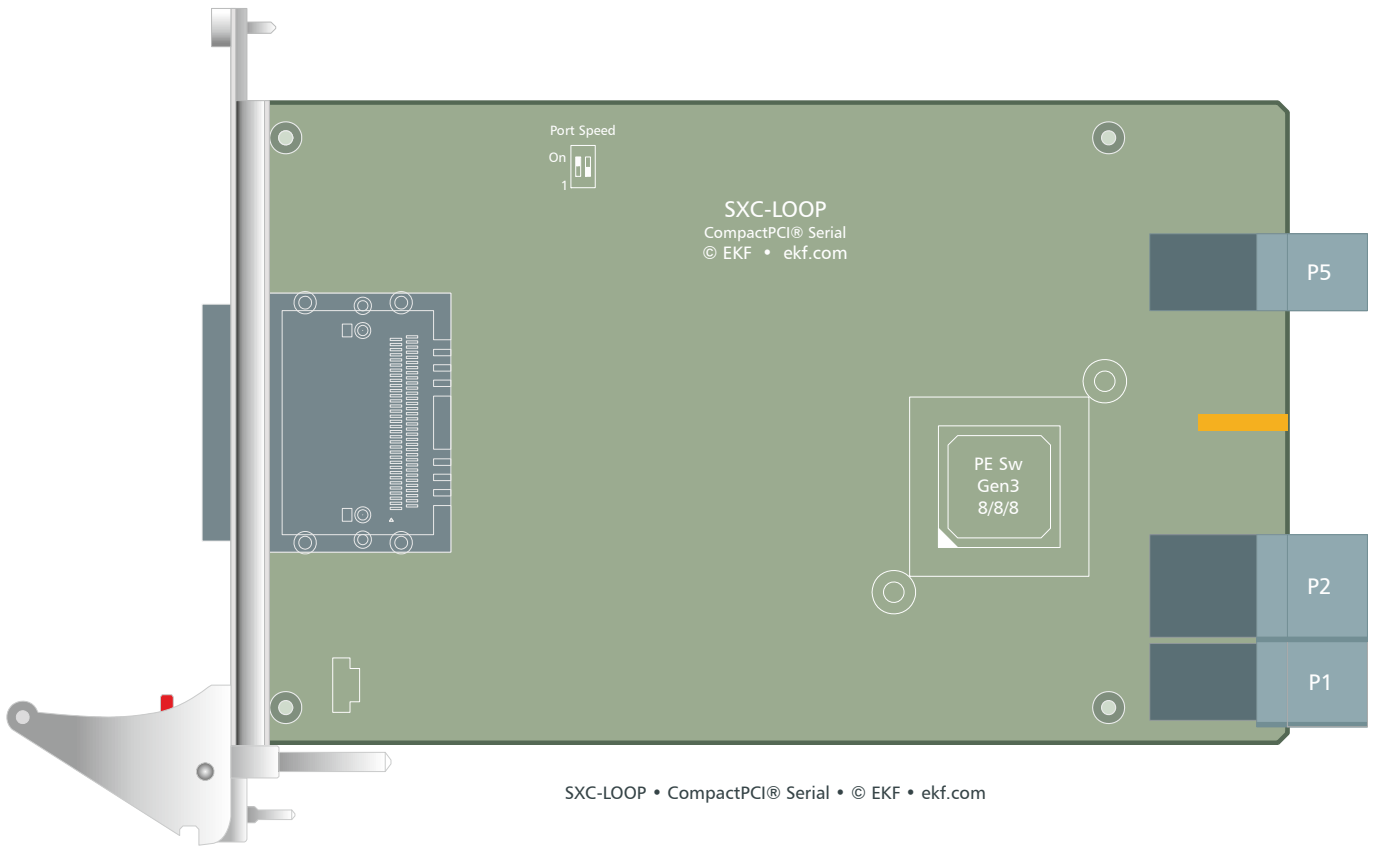
Please note: The front handle is provided with a built-in microswitch, which is used to disable the on-board power circuit when released. Vice versa, the *on-board devices are enabled not before the handle gets locked*. Please refer to the illustration below and make sure that the eject lever has reached its final position for proper board operation, as shown in picture 8. A gentle click should be audible, when the red actuator pin moves into its raised position, indicating that the board is locked and ready for use.



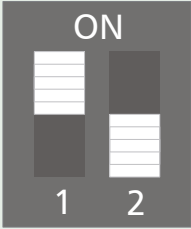
1 - 4: remove board
5 - 8: install board

1 & 8: on-board power enabled
2-7: on-board power disabled

Component Assembly

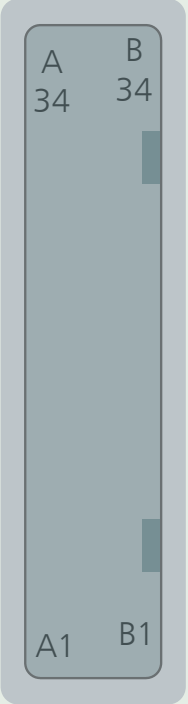


Cable Port Setup

On-Board DIP Switch EKF Part 160.15.02.0			
	Maximum Link Speed		
	1	ON	PCIe® Gen 3 (8GTps)
	2	OFF	
	1	OFF	PCIe® Gen 2 (5GTps)
	2	OFF	
	1	X	PCIe® Gen 1 (2.5GTps)
	2	ON	

By default, this Dip-switch should be set to 1=on, 2=off for up to PCIe® Gen 3 (8GTps), depending on the link training after reset. For testing purposes the cable port transfer speed can be limited to a maximum of PCIe® Gen 2 (5GTps), and even PCIe® Gen 1 (2.5GTps).


PCIe® x8 Cable Connector

Front Panel Connector PCIe® x8				
Pin Numbers A1-17, B1-17				
EKF Parts #255.3.4.068.00 (Receptacle) & 255.3.4.168.00 (Guide Frame)				
 <p>Part #255.3.4.068.00 & 255.3.4.168.00 draft - do not scale • © EKF • ekf.com</p>	GND	A1	B1	GND
	PETp0	A2	B2	PERp0
	PETn0	A3	B3	PERn0
	GND	A4	B4	GND
	PETp1	A5	B5	PERp1
	PETn1	A6	B6	PERn1
	GND	A7	B7	GND
	PETp2	A8	B8	PERp2
	PETn2	A9	B9	PERn2
	GND	A10	B10	GND
	PETp3	A11	B11	PERp3
	PETn3	A12	B12	PERn3
	GND	A13	B13	GND
	CREFLKp	A14	B14	PWR +3.3V
	CREFLKn	A15	B15	PWR +3.3V
	GND	A16	B16	PWR +3.3V
	RSVD	A17	B17	PWR_RTN 1)

PWR +3.3V - protected by on-board PolyFuse 2.0A

For signal descriptions please refer to PCI Express External Cabling Specification Rev. 2.0

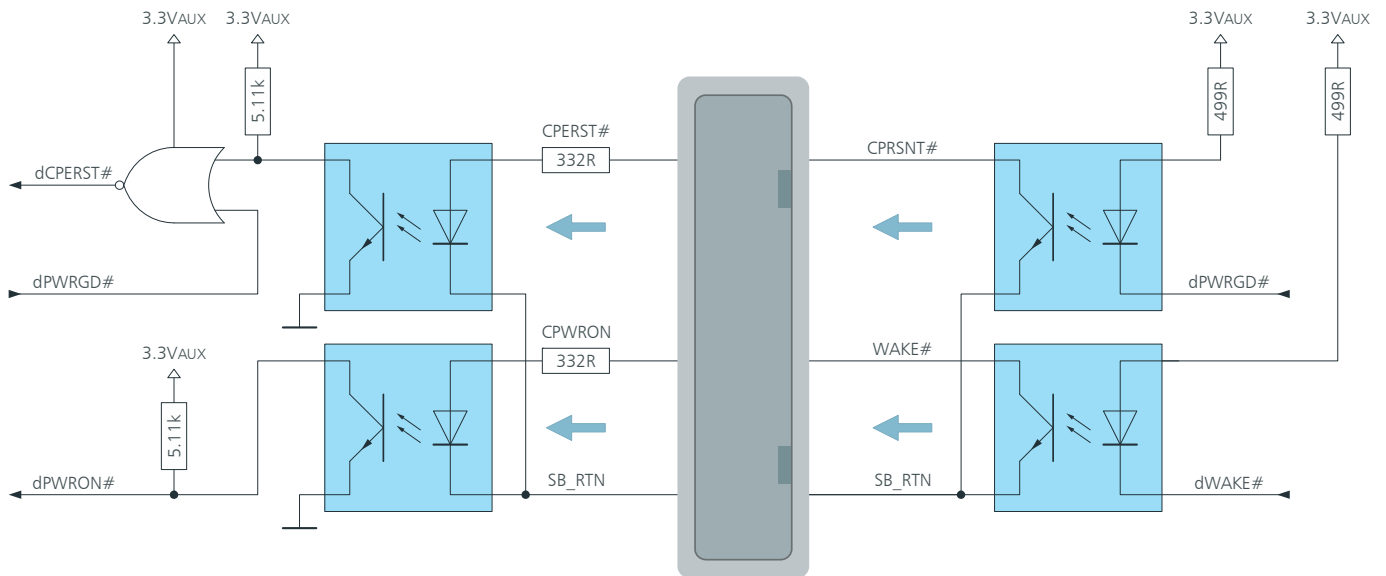
- 1) connected to GND

Front Panel Connectors PCIe® x8				
Pin Numbers A18-34, B18-34				
EKF Parts #255.3.4.068.00 (Receptacle) & 255.3.4.168.00 (Guide Frame)				
 <p>Part #255.3.4.068.00 & 255.3.4.168.00 draft - do not scale • © EKF • ekf.com</p>	RSVD	A18	B18	PWR_RTN 1)
	SB_RTN 2)	A19	B19	PWR_RTN 1)
	CPRSNT# 3)	A20	B20	CWAKE# 3)
	CPWRON 4)	A21	B21	CPERST# 4)
	GND	A22	B22	GND
	PETp4	A23	B23	PERp4
	PETn4	A24	B24	PERn4
	GND	A25	B25	GND
	PETp5	A26	B26	PERp5
	PETn5	A27	B27	PERn5
	GND	A28	B28	GND
	PETp6	A29	B29	PERp6
	PETn6	A30	B30	PERn6
	GND	A31	B31	GND
	PETp7	A32	B32	PERp7
PETn7	A33	B33	PERn7	
GND	A34	B34	GND	

For signal descriptions please refer to PCI Express External Cabling Specification Rev. 2.0

- 1) connected to GND
- 2) Sideband reference GND
- 3) Output to Upstream System (Host) via optocoupler
- 4) Input from Upstream System (Host) via optocoupler

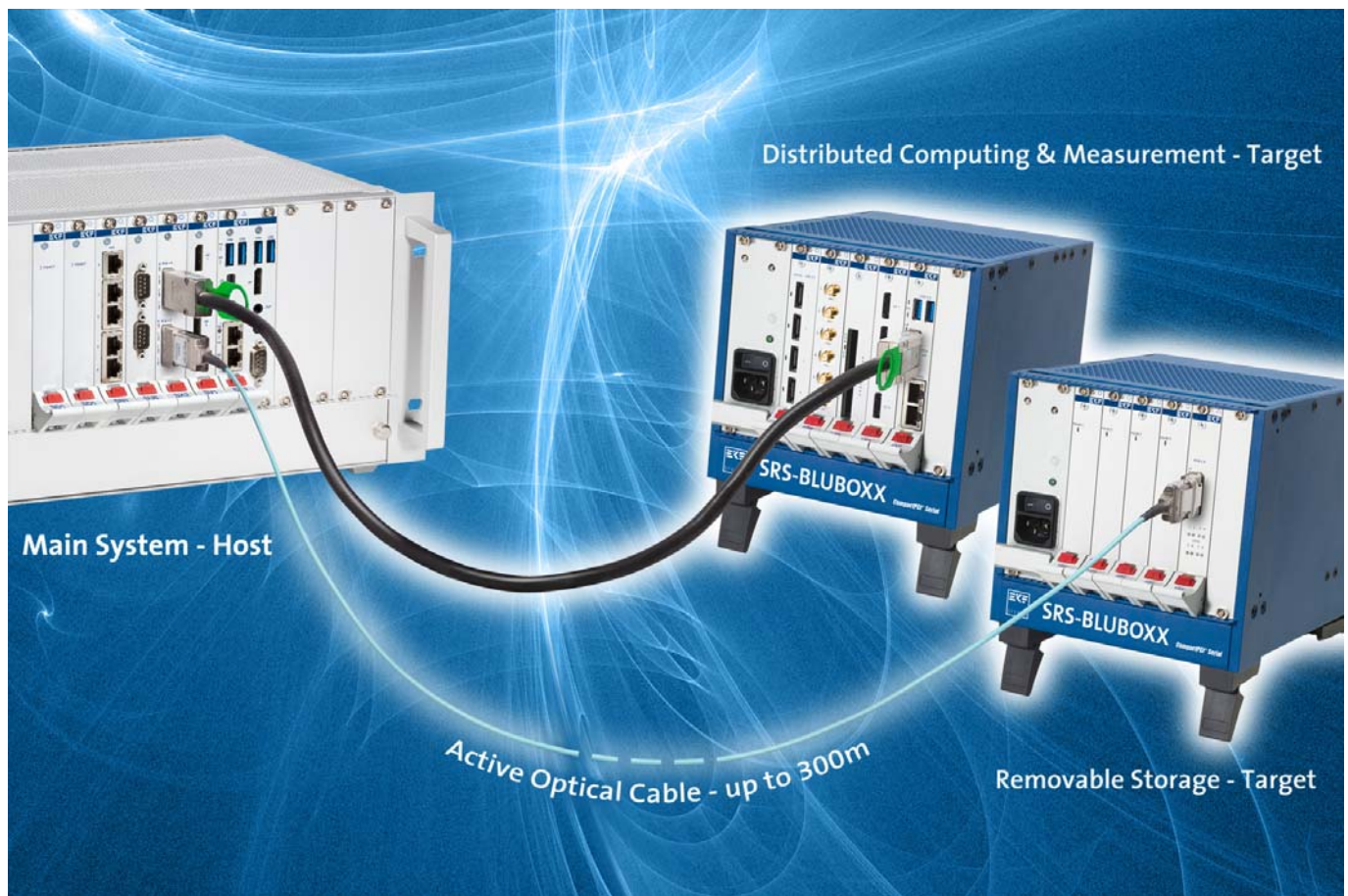
Power-Domain Isolation SX* Target Adapters (Downstream Subsystem) • © EKF



PCIe® Cable Assemblies	
255.3.4.968.0.020	PCIe® x8 external copper cable assembly, 68-circuit, 2m
255.3.4.968.1.020	PCIe® x8 to x4 transition copper cable assembly, 68-circuit, 2m
255.3.4.968.8.0015	PCIe® x8 active optical cable assembly, 1.5m
255.3.4.968.8.0100	PCIe® x8 active optical cable assembly, 10m
255.3.4.968.9.0015	PCIe® x8 to x4 active optical cable assembly, 1.5m
255.3.4.968.9.0100	PCIe® x8 to x4 active optical cable assembly, 10m
other configurations on request	

Particularly helpful for long fiber distances, AOC half cables are available with small MTP™ male or female connectors, to simplify the installation.

Typical Application



For distances up to 300m between host system and target system active optical cables (AOC) are recommended. Below 7m (e.g. when connecting racks in a common enclosure) a low cost copper cable is sufficient. Please note, that an AOC employs a host side connector and a target side connector, which must not be interchanged. A PCI Express® copper cable however is configured identical at both endings. While a copper cable is spread spectrum clock (SSC) compatible, the AOC requires a constant frequency clock (CFC). For proper operation over AOC, setup the host system for CFC.

Power Sequencing

Please understand, that host and connected target hardware should be considered as distributed parts of a common computer system. During BIOS POST the whole system will be explored for PCI Express® devices attached to the PCIe® root complex (processor on host system CPU card). Devices which are not active (powered up) at this time, will not be enumerated by the BIOS and are consequently not available for the operating system afterwards.

Hence a power sequencing procedure must be observed for host system and target system. The rule is simple: **Power up the target system before the host system, or simultaneously.** If power sequencing conditions cannot be maintained, the host system must be restarted again, until the remote target devices are visible to the host CPU.

If the host system is equipped with an EKF processor board such as the SC3-LARGO or later, a startup time delay up to 12s can be configured via BIOS setup:

Setup (F2): Advanced -> Miscellaneous Configuration -> Execute Delay after Reset

The adjusted delay would be executed before enumeration and initialization of PCI Express® devices, thus permitting a reasonable power up time lag for the remote target system. The delay countdown is indicated by a red blinking LED GP in the CPU card front panel.

P1 CompactPCI® Serial System Slot Backplane Connector

P1 CompactPCI® Serial System Slot Backplane Connector												
EKF Part #250.3.1206.20.02 • 72 pos. 12x6, 14mm Width												
P1	A	B	C	D	E	F	G	H	I	J	K	L
6	GND	1_PE TX02+	1_PE TX02-	GND	1_PE RX02+	1_PE RX02-	GND	1_PE TX03+	1_PE TX03-	GND	1_PE RX03+	1_PE RX03-
5	1_PE TX00+	1_PE TX00-	GND	1_PE RX00+	1_PE RX00-	GND	1_PE TX01+	1_PE TX01-	GND	1_PE RX01+	1_PE RX01-	GND
4	GND	1_ USB2+	1_ USB2-	GND	RSV	RSV	GND	1_SAT A TX+	1_SAT A TX-	GND	1_SAT A RX+	1_SAT A RX-
3	1_USB 3 TX+	1_USB 3 TX-	PWR BTN#	1_USB 3 RX+	1_USB 3 RX-	PWR_ FAIL#	SATA SDI	SATA SDO	GND GA2	SATA SCL	SATA SL	GND GA3
2	GND	I2C SCL	I2C SDA	GND	GND PS_ON #	RST#	GND	PRST#	WAKE#	GND	RSV	SYS EN#
1	+12V	STBY	GND	+12V	+12V	GND	+12V	+12V	GND	+12V	+12V	GND

pin positions printed gray: not connected or PU terminated

For signal descriptions please refer to PICMG CPCI-S.0 R1.0 CompactPCI® Serial Specification

P2 CompactPCI® Serial System Slot Backplane Connector

P2 CompactPCI® Serial System Slot Backplane Connector												
EKF Part #250.3.1208.20.00 • 96 pos. 12x8, 16mm Width												
P2	A	B	C	D	E	F	G	H	I	J	K	L
8	GND	IO	IO	GND	2_ USB2+	2_ USB2-	GND	3_ USB2+	3_ USB2-	IO	4_ USB2+	4_ USB2-
7	IO	IO	GND	IO	IO	GND	IO	IO	GND	IO	IO	GND
6	GND	2_PE TX06+	2_PE TX06-	GND	2_PE RX06+	2_PE RX06-	GND	2_PE TX07+	2_PE TX07-	GND	2_PE RX07+	2_PE RX07-
5	2_PE TX04+	2_PE TX04-	GND	2_PE RX04+	2_PE RX04-	GND	2_PE TX05+	2_PE TX05-	GND	2_PE RX05+	2_PE RX05-	GND
4	GND	2_PE TX02+	2_PE TX02-	GND	2_PE RX02+	2_PE RX02+	GND	2_PE TX03+	2_PE TX03-	GND	2_PE RX03+	2_PE RX03-
3	2_PE TX00+	2_PE TX00-	GND	2_PE RX00+	2_PERX 00-	GND	2_PE TX01+	2_PE TX01-	GND	2_PE RX01+	2_PE RX01-	GND
2	GND	1_PE TX06+	1_PE TX06-	GND	1_PE RX06+	1_PE RX06-	GND	1_PE TX07+	1_PE TX07-	GND	1_PE RX07+	1_PE RX07-
1	1_PE TX04+	1_PE TX04-	GND	1_PE RX04+	1_PE RX04-	GND	1_PE TX05+	1_PE TX05-	GND	1_PE RX05+	1_PE RX05-	GND

pin positions printed gray: not connected or PU terminated

For signal descriptions please refer to PICMG CPCI-S.0 R1.0 CompactPCI® Serial Specification

P5 CompactPCI® Serial System Slot Backplane Connector

P5 CompactPCI® Serial System Slot Backplane Connector												
EKF Part #250.3.1206.20.00 • 72 pos. 12x6, 12mm Width												
P5	A	B	C	D	E	F	G	H	I	J	K	L
6	5_PE	5_PE	5_PE	6_PE	6_PE	6_PE	7_PE	7_PE	7_PE	8_PE	8_PE	8_PE
	CLKE#	CLK+	CLK-	CLKE#	CLK+	CLK-	CLKE#	CLK+	CLK-	CLKE#	CLK+	CLK-
5	1_PE	1_PE	1_PE	2_PE	2_PE	2_PE	3_PE	3_PE	3_PE	4_PE	4_PE	4_PE
	CLK+	CKL-	CLKE#	CLK+	CKL-	CLKE#	CLK+	CKL-	CLKE#	CLK+	CKL-	CLKE#
4	GND	8_PE TX02+	8_PE TX02-	GND	8_PE RX02+	8_PE RX02-	GND	8_PE TX03+	8_PE TX03-	GND	8_PE RX03+	8_PE RX03-
3	8_PE TX00+	8_PE TX00-	GND	8_PE RX00+	8_PE RX00-	GND	8_PE TX01+	8_PE TX01-	GND	8_PE RX01+	8_PE RX01-	GND
2	GND	7_PE TX02+	7_PE TX02-	GND	7_PE RX02+	7_PE RX02-	GND	7_PE TX03+	7_PE TX03-	GND	7_PE RX03+	7_PE RX03-
1	7_PE TX00+	7_PE TX00-	GND	7_PE RX00+	7_PE RX00-	GND	7_PE TX01+	7_PE TX01-	GND	7_PE RX01+	7_PE RX01-	GND

pin positions printed gray: not connected

For signal descriptions please refer to PICMG CPCI-S.0 R1.0 CompactPCI® Serial Specification

Related Documents

Similar Cards Using PCIe External Cabling	
SX2-SLIDE	CompactPCI® Serial • Host Side Dual Gen2 x4 www.ekf.com/s/sx2/sx2.html
SX5-STREAM	CompactPCI® Serial • Host Side Dual Gen3 x8 www.ekf.com/s/sx5/sx5.html
SX6-FIREWORKS	CompactPCI® Serial • Host Side Dual Gen3 x8 MPO/MTP Optical Cable Connectors www.ekf.com/s/sx6/sx6.html
SX9-HOWL	CompactPCI® Serial • Target Side Gen2 x4 • PCIe System Slot Replicator www.ekf.com/s/sx9/sx9.html
SXD-FIREWORKS	CompactPCI® Serial • Target Side Gen3 x8 MPO/MTP Optical Cable Connectors www.ekf.com/s/sxd/sxd.html
SXS-STRING	CompactPCI® Serial • Target Side Gen2 x4 • 8-Port SATA RAID www.ekf.com/s/sxs/sxs.html
DC2-STAG	XMC Mezzanine Module • Host Side Dual Gen2 x4 www.ekf.com/d/dpxc/dc2/dc2.html

Reference Documents		
Term	Document	Origin
CompactPCI® Serial	CPCI-S.0	www.picmg.org
PCI Express®	PCI Express® External Cabling Specification 2.0	www.pcisig.com

Ordering Information

Ordering Information

For popular SXC-LOOP SKUs please refer to www.ekf.com/liste/liste_21.html#SXC





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